

# 700V GaN Power Transistor (FET)

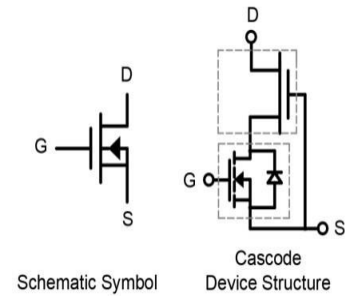
## Features

- Easy to use, compatible with standard gate drivers
- Excellent  $Q_G \times R_{DS(on)}$  figure of merit (FOM)
- Low  $Q_{RR}$ , no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

Product Summary		
$V_{DSS}$	700	V
$R_{DS(on), typ}$	240	mΩ
$Q_G, typ$	6	nC
$Q_{RR, typ}$	27	nC

## Applications

- High efficiency power supplies
- High efficiency USB PD adapters
- Other consumer electronics



## Packaging

Part Number	Package	Packaging	Base QTY
JZ70T240DSL	2 Lead TO-252	Tape and Reel	2500

## Maximum ratings, at $T_C=25^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter		Limit Value	Unit
$I_D$	Continuous drain current @ $T_C=25^\circ\text{C}$		8.1	A
	Continuous drain current @ $T_C=100^\circ\text{C}$		5.1	A
$I_{DM}$	Pulsed drain current @ $T_C=25^\circ\text{C}$ (pulse width: 100us)		19	A
	Pulsed drain current @ $T_C=150^\circ\text{C}$ (pulse width: 100us)		15	A
$V_{DSS}$	Drain to source voltage ( $T_J = -55^\circ\text{C}$ to $150^\circ\text{C}$ )		700	V
$V_{TDSS}$	Transient drain to source voltage <sup>a</sup>		800	V
$V_{GSS}$	Gate to source voltage		±20	V
$P_D$	Maximum power dissipation @ $T_C=25^\circ\text{C}$		30	W
$T_C$	Operating temperature	Case	-55 to 150	°C
$T_J$		Junction	-55 to 150	°C
$T_S$	Storage temperature		-55 to 150	°C
$T_{CSOLD}$	Soldering peak temperature		260	°C

**Thermal Resistance**

Symbol	Parameter	Typical	Unit
R <sub>θJC</sub>	Junction-to-case	4.2	°C/W
R <sub>θJA</sub>	Junction-to-ambient <sup>b</sup>	50	°C/W

## Notes:

a. Off-state spike duty cycle &lt; 0.01, spike duration &lt; 2us

b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm<sup>2</sup>copper area and 70μm thickness)

**Electrical Parameters, at  $T_J=25^\circ\text{C}$ , unless otherwise specified**

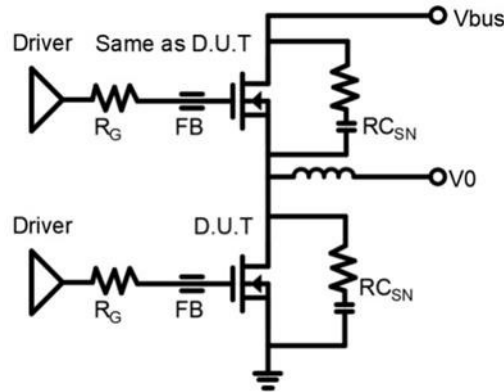
Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Characteristics					
$V_{DSS-MAX}$	700	-	-	V	$V_{GS}=0V$
$BV_{DSS}$	-	1000	-		$V_{GS}=0V, I_{DSS}=250\mu A$
$V_{GS(th)}$	1.1	1.8	2.5	V	$V_{DS}=V_{GS}, I_D=500\mu A$
$R_{DS(on)}^c$	-	240	300	mΩ	$V_{GS}=8V, I_D=4A, T_J=25^{\circ}C$
	-	480	-		$V_{GS}=8V, I_D=4A, T_J=150^{\circ}C$
$I_{DSS}$	-	5	20	μA	$V_{DS}=700V, V_{GS}=0V, T_J=25^{\circ}C$
	-	50	-	μA	$V_{DS}=700V, V_{GS}=0V, T_J=150^{\circ}C$
$I_{GSS}$	-	-	150	nA	$V_{GS}=20V$
	-	-	-150	nA	$V_{GS}=-20V$
$C_{ISS}$	-	277	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1MHz$
$C_{OSS}$	-	15	-	pF	
$C_{RSS}$	-	0.6	-	pF	
$C_{O(er)}$	-	22	-	pF	$V_{GS}=0V, V_{DS}=0 - 400V$
$C_{O(tr)}$	-	67	-	pF	
$Q_{OSS}$	-	27	-	nC	
$Q_G$	-	6	-	nC	$V_{DS}=400V, V_{GS}=0 - 8V, I_D=5A$
$Q_{GS}$	-	1.5	-		
$Q_{GD}$	-	2.5	-		
$t_{D(on)}$	-	28	-	ns	$V_{DS}=400V, V_{GS}=0 - 12V, I_D=4A, R_G=47\Omega$
$t_R$	-	14	-		
$t_{D(off)}$	-	108	-		
$t_F$	-	8	-		
Reverse Characteristics					
$V_{SD}$	-	1.4	-	V	$V_{GS}=0V, I_S=2.5A, T_J=25^{\circ}C$
	-	2.1	-		$V_{GS}=0V, I_S=5A, T_J=25^{\circ}C$
	-	3.3	-		$V_{GS}=0V, I_S=5A, T_J=150^{\circ}C$
$t_{RR}$	-	16	-	ns	$I_S=5A, V_{GS}=0V, d_i/d_t=1000A/us, V_{DD}=400V$
$Q_{RR}$	-	27	-	nC	

Notes:

c. Dynamic on-resistance; see Figure 19 and 20 for test circuit and configurations

## Circuit Implementation

- (1) Mostly used in half bridge and full bridge topology



**Recommended Half-bridge Circuit**

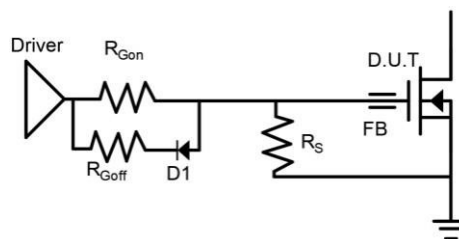
Recommended gate drive: (0 V, 8 V) with  $R_{G(tot)} = 40 \Omega$ , where  $R_{G(tot)} = R_G + R_{driver}$

Gate Ferrite Bead (FB)	Gate Resistance ( $R_G$ )	RC Snubber ( $R_{CSN}$ )
MPZ1608S471ATA00	33 $\Omega$	69 pF + 15 $\Omega$

Notes:

- d.  $R_{CSN}$  should be placed as close as possible to the drain pin
- e. The layout and wiring of the drive circuit should be as short as possible

- (2) Mostly used in flyback, forward and push-pull converters

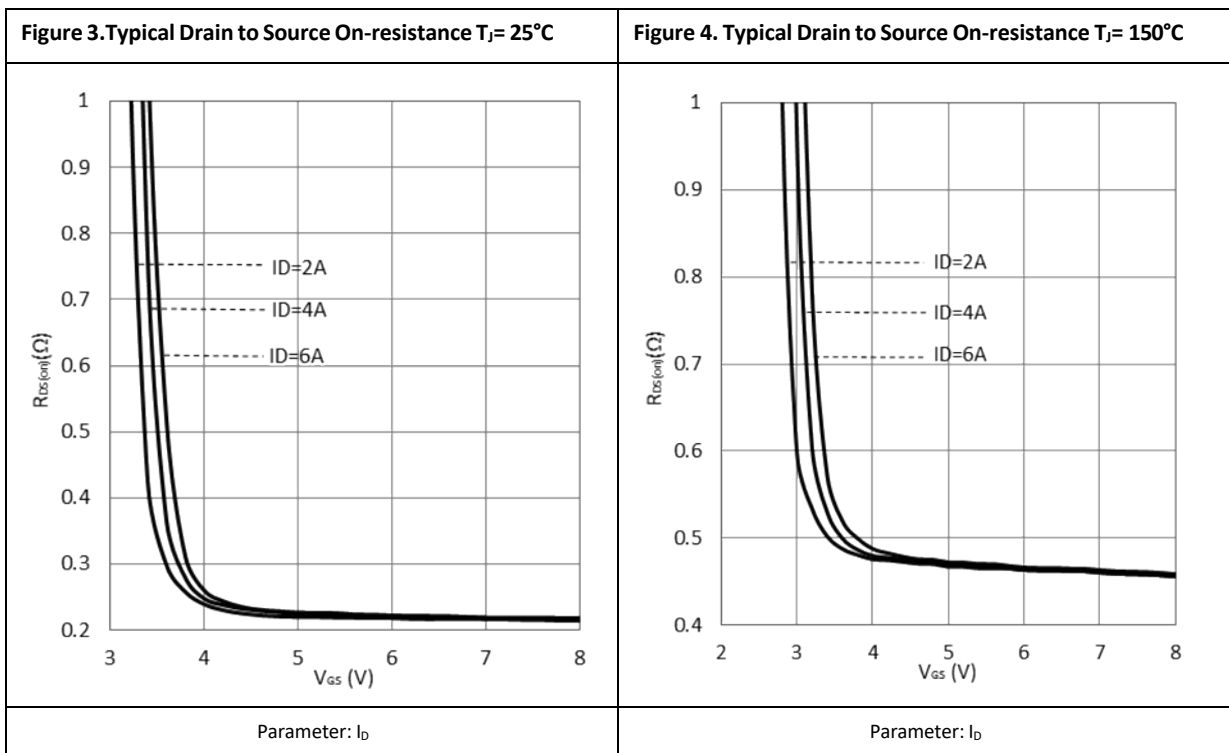
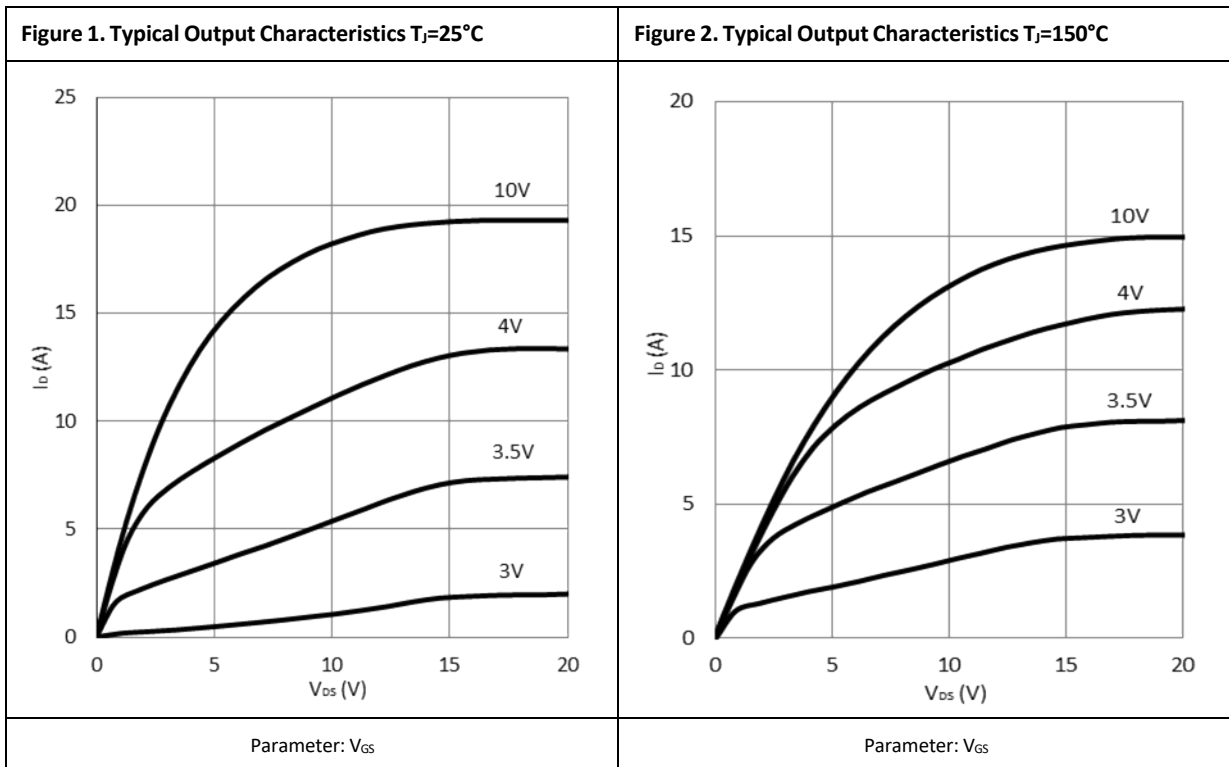


**Recommended Single Ended Drive Circuit**

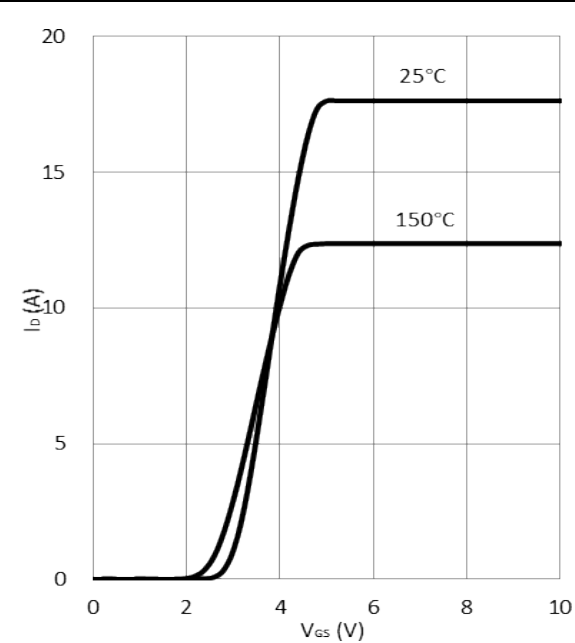
Recommended gate drive: (0 V, 12 V) with  $R_{Gon} = 300 - 500 \Omega$ ,  $R_{Goff} = 10 \Omega$

Gate Ferrite Bead (FB)	Gate Source Resistance ( $R_S$ )	Gate Diode (D1)
300 - 600 $\Omega$ @100MHz	10 k $\Omega$	1N4148

Typical Characteristics, at  $T_c=25^\circ\text{C}$ , unless otherwise specified

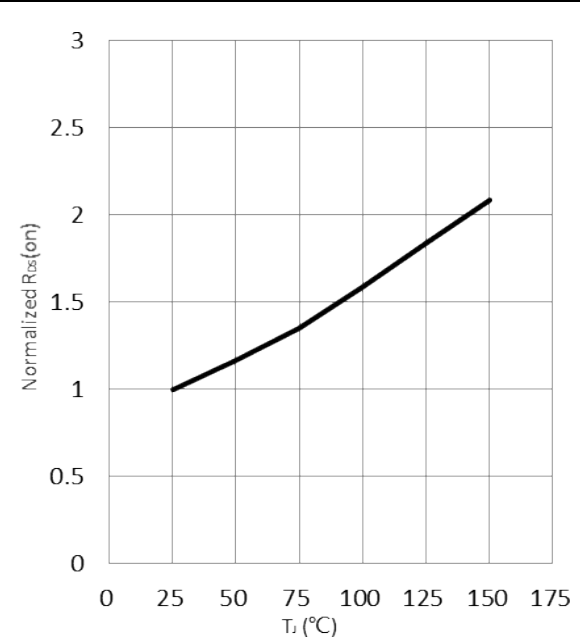


**Figure 5. Typical Transfer Characteristics**



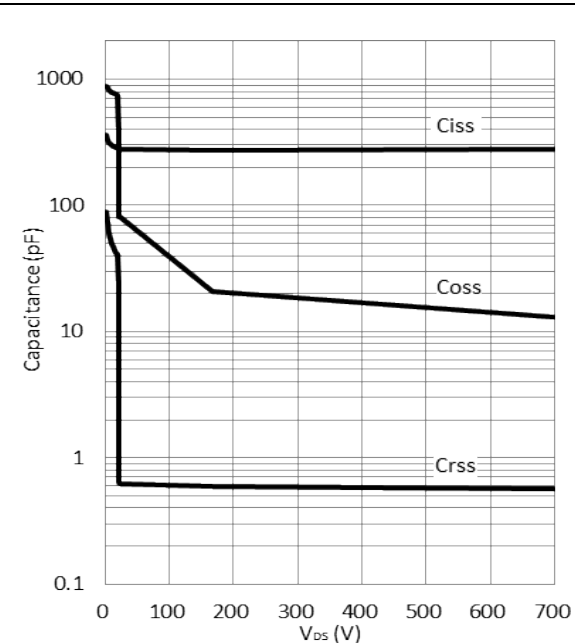
V<sub>DS</sub>=10V, Parameter: T<sub>J</sub>

**Figure 6. Normalized On-resistance**



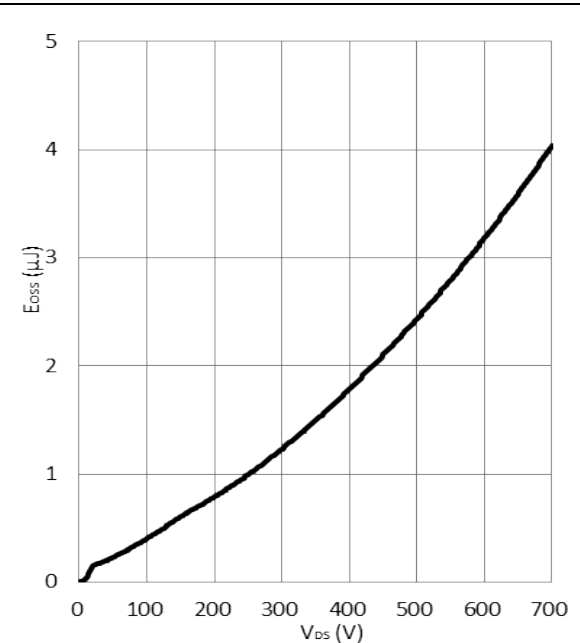
I<sub>D</sub>=4A, V<sub>GS</sub>=8V

**Figure 7. Typical Capacitance**



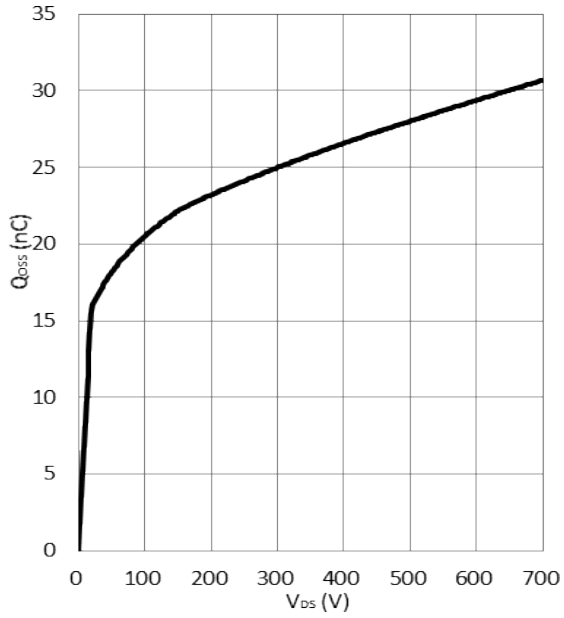
V<sub>GS</sub>=0V, f=1MHz

**Figure 8. Typical Coss Stored Energy**



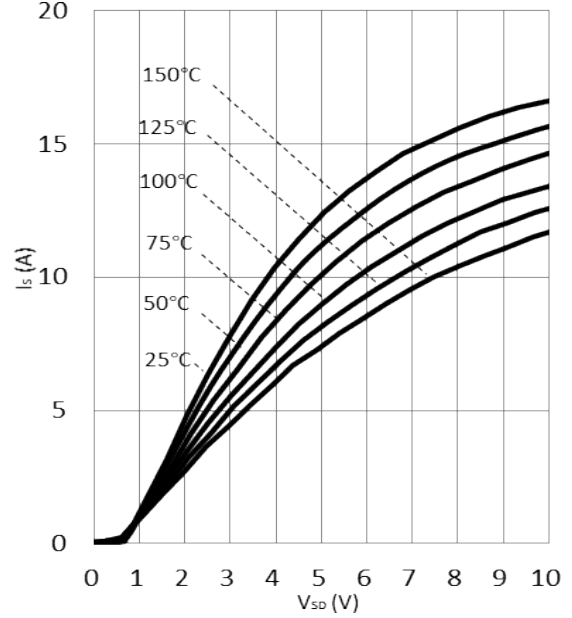
V<sub>GS</sub>=0V, f=1MHz

**Figure 9. Typical Qoss**



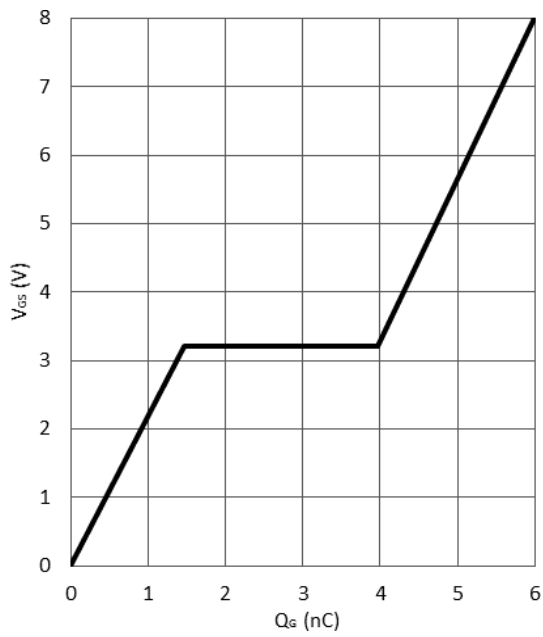
VGS=0V, f=1MHz

**Figure 10. Forward Characteristic of Rev. Diode**



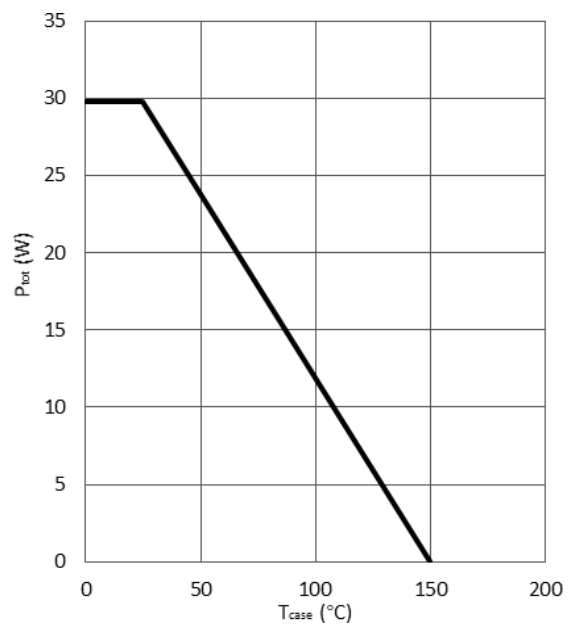
IS=f(VSD), Parameter TJ

**Figure 11. Typical Gate Charge**

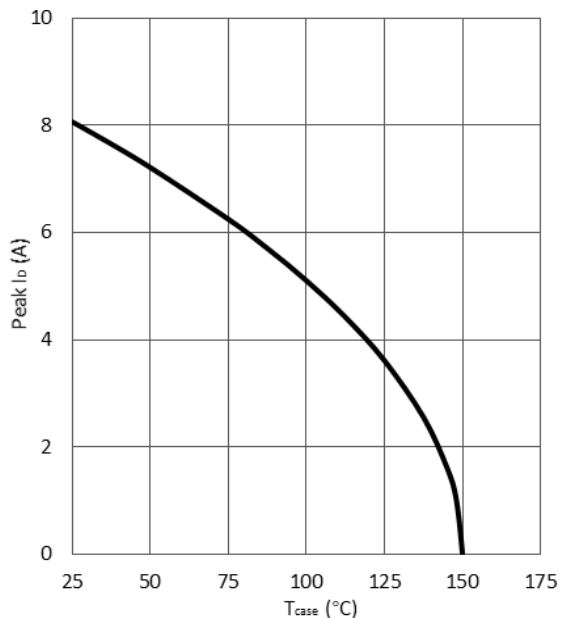


IDS=5A, VDS=400V

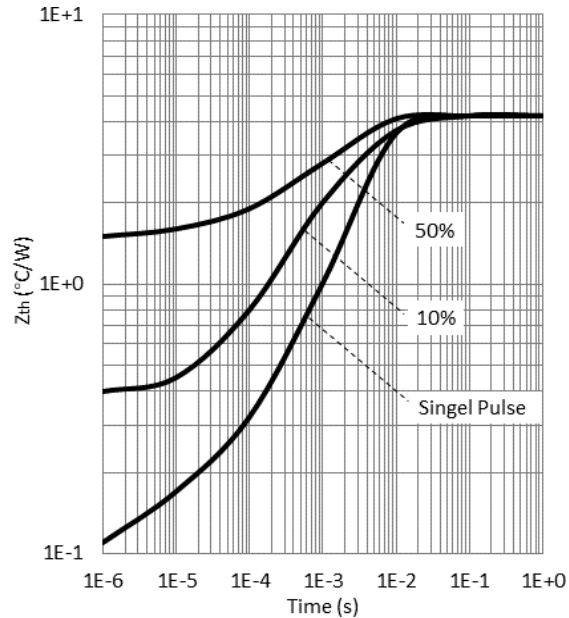
**Figure 12. Power Dissipation**



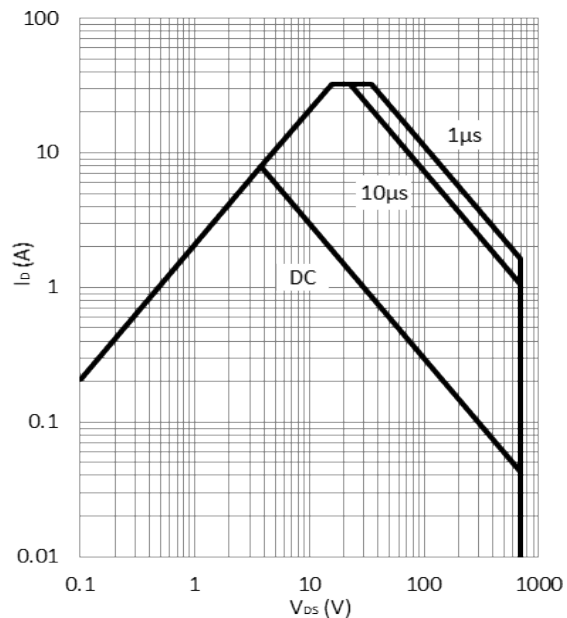
**Figure 13. Current Derating**



**Figure 14. Transient Thermal Resistance**

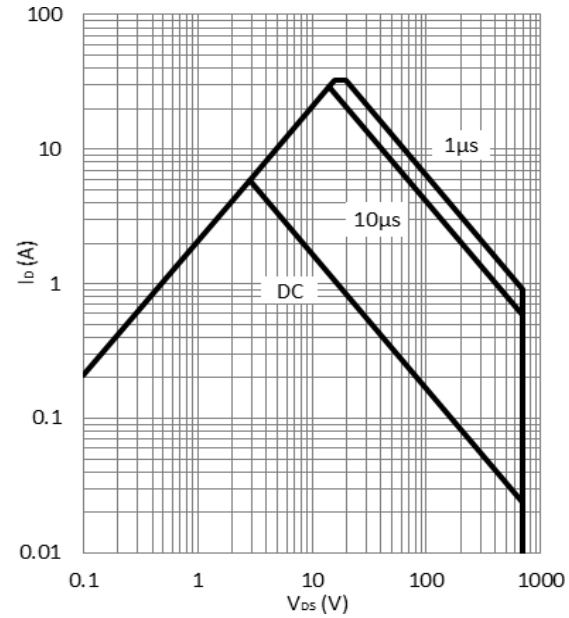


**Figure 15. Safe Operating Area T<sub>C</sub>=25°C**



calculated based on thermal limit

**Figure 16. Safe Operating Area T<sub>C</sub>=80°C**



calculated based on thermal limit



### Test Circuits and Waveforms

Figure 17. Switching Time Test Circuit

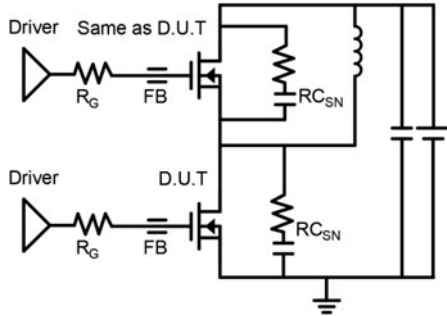


Figure 18. Switching Time Waveform

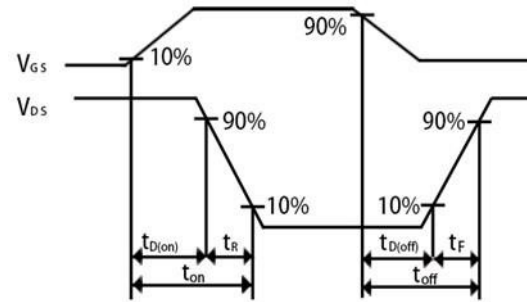


Figure 19. Dynamic R\_DS(on) Test Circuit

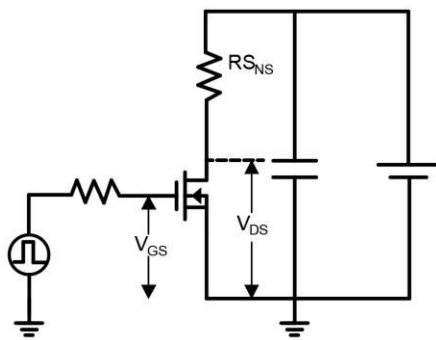


Figure 20. Dynamic R\_DS(on) Waveform

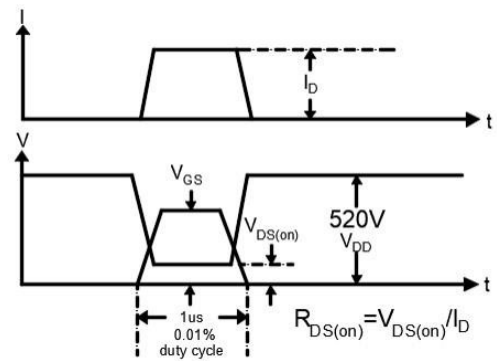


Figure 21. Diode Characteristic Test Circuits

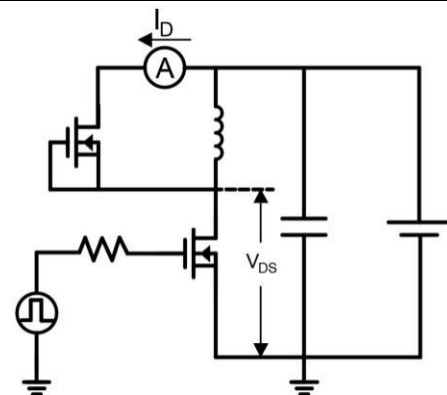
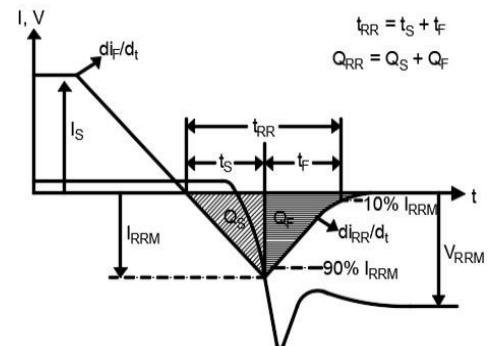


Figure 22. Diode Recovery Waveform



**Design Considerations**

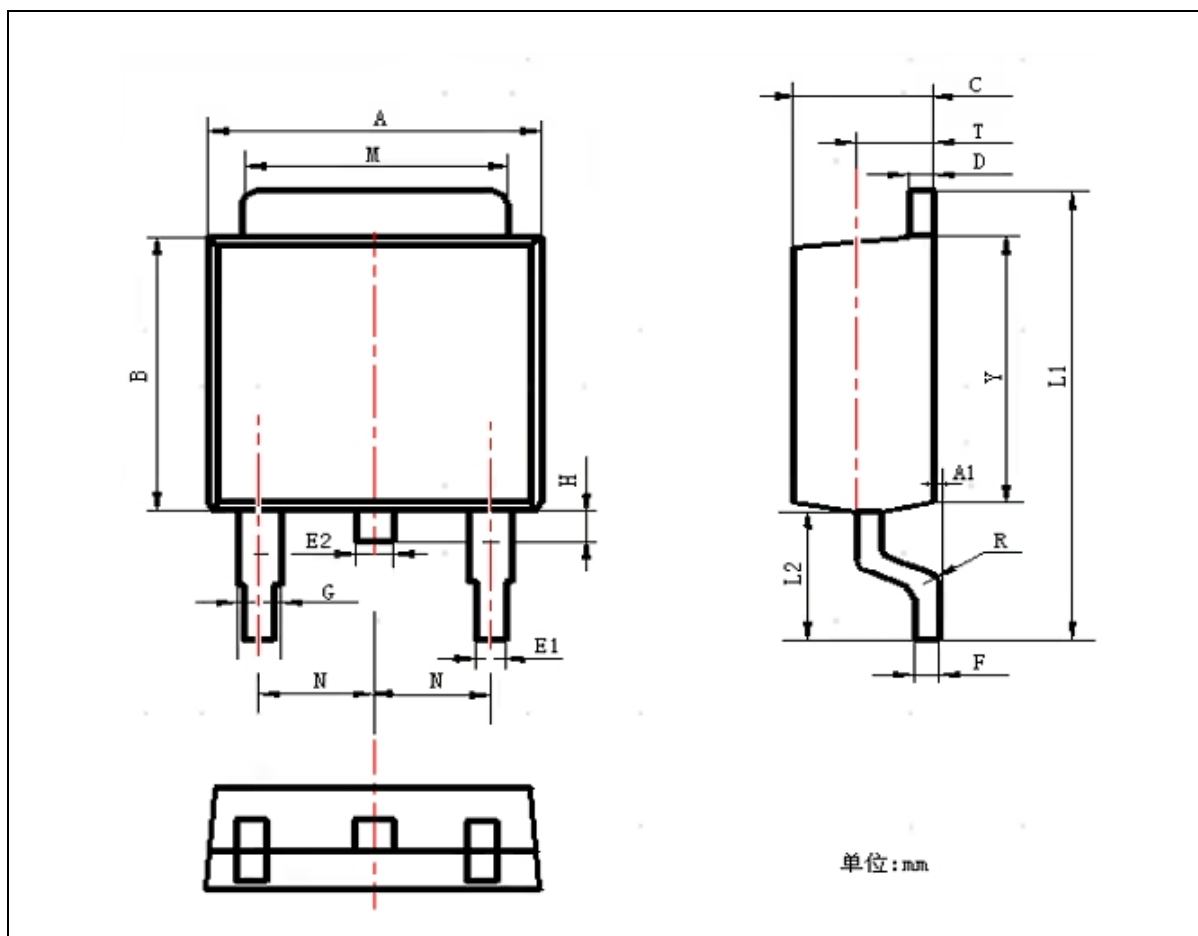
Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

Before evaluating Runxin Micro's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

**When Evaluating Runxin Micro's GaN Devices:**

<b>DO</b>	<b>DO NOT</b>
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Runxin Micro's devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of DFN 8*8mm packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

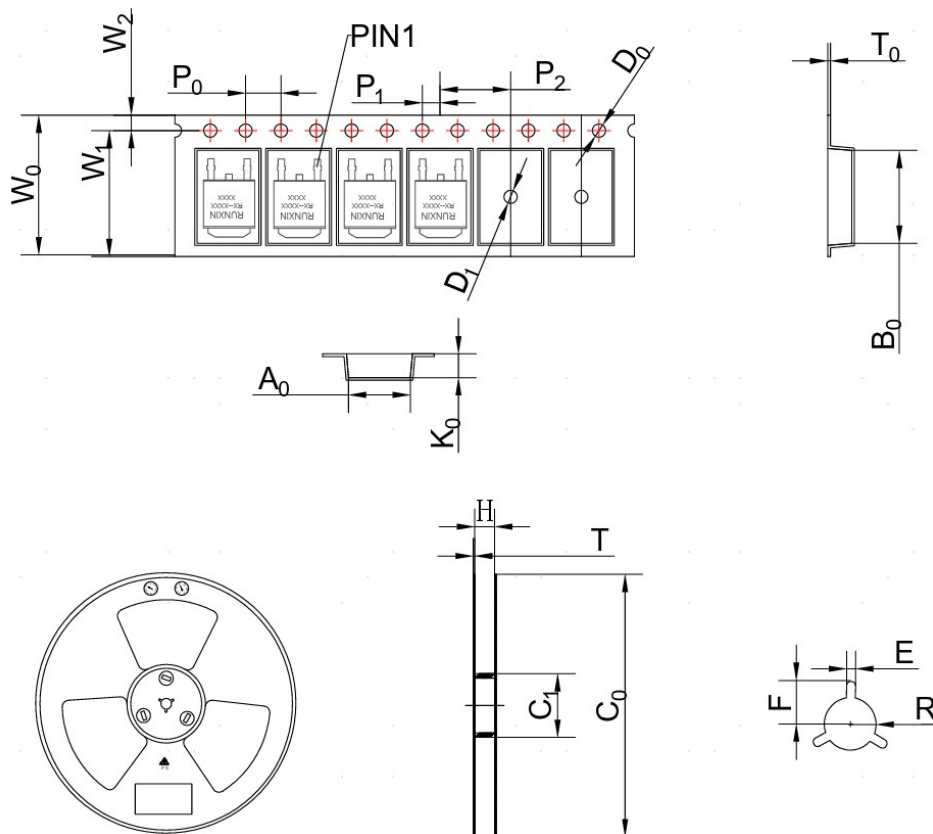
## Package Outline



SYMBOL	Millimeter		
	Min	Nom	Max
A	6.30	6.60	6.90
A1	0	0.80	0.16
B	5.70	6.00	6.30
C	2.10	2.30	2.50
D	0.30	0.60	0.90
E1	0.60	0.75	0.90
F	0.30	0.45	0.60
G	0.70	0.95	1.20
L1	9.30	9.90	10.50
L2	2.50	2.80	3.10
H	0.40	0.70	1.05
M	4.90	5.30	5.60
N	2.09	2.29	2.49

### Tape and Reel Information

Dimensions are shown in millimeters

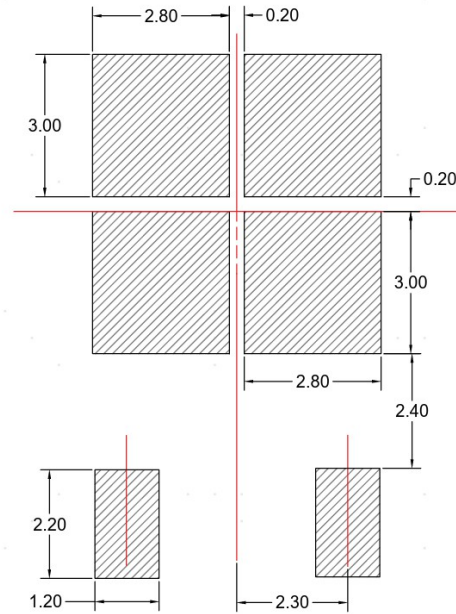
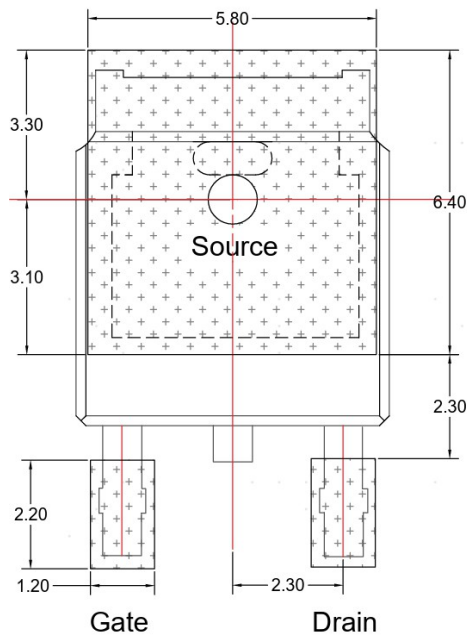


Tape Dimension(mm)					
W <sub>0</sub>	16+0.3-0.2	P <sub>0</sub>	4±0.1	A <sub>0</sub>	7±0.1
W <sub>1</sub>	14.25±0.1	P <sub>1</sub>	2±0.1	B <sub>0</sub>	10.5±0.1
W <sub>2</sub>	1.75±0.1	P <sub>2</sub>	8±0.1	D <sub>1</sub>	1.5±0.25
K <sub>0</sub>	2.7±0.1	D <sub>0</sub>	1.5±0.1	T <sub>0</sub>	0.3±0.05

Reel Dimension(mm)			
H	17±0.1	F	10.5±0.1
T	2±0.2	E	2.8±0.1
C <sub>0</sub>	330±3	R	6.5±0.1
C <sub>1</sub>	100±1		

**Recommended PCB Layout & Stencil apertures**

Dimensions are shown in millimeters



Chip electrodes



PCB layout



Stencil aperture

**Revision History**

Version	Date	Change(s)
0.1	2024/10/16	Release preliminary datasheet

**Disclaimer**

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.